DACSINE PAGE 1

1 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

2 ;

3 ; Author : ADI - Apps www.analog.com/MicroConverter

4 ;

5 ; Date : 28 May 1999

6 ;

7 ; File : DACsine.asm

8 ;

9 ; Hardware : ADuC812

10 ;

11 ; Description : Outputs a sine waves on DAC0 at 720Hz.

12 ; Rate calculations assume an 11.0592MHz Mclk.

13 ;

14 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

15

16 $MOD812 ; Use 8052&ADuC812 predefined symbols

17

00B4 18 LED EQU P3.4 ; P3.4 drives red LED on eval board

19

20 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

21 ; BEGINNING OF CODE

---- 22 CSEG

23

0000 24 ORG 0000h

25

0000 75FD0D 26 MOV DACCON,#00Dh ; DAC0 on, 12bit, asynchronous

0003 75FA08 27 MOV DAC0H,#008h

0006 75F900 28 MOV DAC0L,#000h ; DAC0 to mid-scale

29

0009 901000 30 MOV DPTR,#TABLE

31

000C E4 32 STEP: CLR A ; 1

000D 93 33 MOVC A,@A+DPTR ; get high data byte from table.. 2

000E F5FA 34 MOV DAC0H,A ; ..and move it into DAC register 1

0010 A3 35 INC DPTR ; move on to get low byte 2

36

0011 E4 37 CLR A ; 1

0012 93 38 MOVC A,@A+DPTR ; get low data byte from table.. 2

0013 F5F9 39 MOV DAC0L,A ; ..and update DAC output 1

0015 A3 40 INC DPTR ; move on for next data point 2

41

0016 53827F 42 ANL DPL,#07Fh ; wrap around at end of table 2

43

0019 E5FA 44 MOV A,DAC0H ; 1

001B A2E3 45 MOV C,ACC.3 ; MSB of DAC0 value 1

001D 92B4 46 MOV LED,C ; LED = MSB of DAC0 2

47

001F 80EB 48 JMP STEP ; 2

49

50 ; numbers at right in the above loop represent the number of machine

51 ; cycles for each instruction. the complete loop takes exactly 20

52 ; machine cycles. with an 11.0592MHz master clock, a machine cycle

53 ; is 1.085us, so the above loop takes 21.70us to update each data

54 ; point. since there are 64 data points in the below sine lookup

55 ; table, this results in a 1.389ms period, i.e. a 720.0Hz frequency.

56

57 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

58 ; SINE LOOKUP TABLE

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1000 59 ORG 01000h

60

1000 61 TABLE:

62

1000 07FF 63 DB 007h, 0FFh

1002 08C8 64 DB 008h, 0C8h

1004 098E 65 DB 009h, 08Eh

1006 0A51 66 DB 00Ah, 051h

1008 0B0F 67 DB 00Bh, 00Fh

100A 0BC4 68 DB 00Bh, 0C4h

100C 0C71 69 DB 00Ch, 071h

100E 0D12 70 DB 00Dh, 012h

1010 0DA7 71 DB 00Dh, 0A7h

1012 0E2E 72 DB 00Eh, 02Eh

1014 0EA5 73 DB 00Eh, 0A5h

1016 0F0D 74 DB 00Fh, 00Dh

1018 0F63 75 DB 00Fh, 063h

101A 0FA6 76 DB 00Fh, 0A6h

101C 0FD7 77 DB 00Fh, 0D7h

101E 0FF5 78 DB 00Fh, 0F5h

1020 0FFF 79 DB 00Fh, 0FFh

1022 0FF5 80 DB 00Fh, 0F5h

1024 0FD7 81 DB 00Fh, 0D7h

1026 0FA6 82 DB 00Fh, 0A6h

1028 0F63 83 DB 00Fh, 063h

102A 0F0D 84 DB 00Fh, 00Dh

102C 0EA5 85 DB 00Eh, 0A5h

102E 0E2E 86 DB 00Eh, 02Eh

1030 0DA7 87 DB 00Dh, 0A7h

1032 0D12 88 DB 00Dh, 012h

1034 0C71 89 DB 00Ch, 071h

1036 0BC4 90 DB 00Bh, 0C4h

1038 0B0F 91 DB 00Bh, 00Fh

103A 0A51 92 DB 00Ah, 051h

103C 098E 93 DB 009h, 08Eh

103E 08C8 94 DB 008h, 0C8h

1040 07FF 95 DB 007h, 0FFh

1042 0736 96 DB 007h, 036h

1044 0670 97 DB 006h, 070h

1046 05AD 98 DB 005h, 0ADh

1048 04EF 99 DB 004h, 0EFh

104A 043A 100 DB 004h, 03Ah

104C 038D 101 DB 003h, 08Dh

104E 02EC 102 DB 002h, 0ECh

1050 0257 103 DB 002h, 057h

1052 01D0 104 DB 001h, 0D0h

1054 0159 105 DB 001h, 059h

1056 00F1 106 DB 000h, 0F1h

1058 009B 107 DB 000h, 09Bh

105A 0058 108 DB 000h, 058h

105C 0027 109 DB 000h, 027h

105E 0009 110 DB 000h, 009h

1060 0000 111 DB 000h, 000h

1062 0009 112 DB 000h, 009h

1064 0027 113 DB 000h, 027h

1066 0058 114 DB 000h, 058h

1068 009B 115 DB 000h, 09Bh

106A 00F1 116 DB 000h, 0F1h

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106C 0159 117 DB 001h, 059h

106E 01D0 118 DB 001h, 0D0h

1070 0257 119 DB 002h, 057h

1072 02EC 120 DB 002h, 0ECh

1074 038D 121 DB 003h, 08Dh

1076 043A 122 DB 004h, 03Ah

1078 04EF 123 DB 004h, 0EFh

107A 05AD 124 DB 005h, 0ADh

107C 0670 125 DB 006h, 070h

107E 0736 126 DB 007h, 036h ; end of table

127

128 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

129

130 END

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

DACSINE PAGE 4

ACC. . . . . . . . . . . . . . . D ADDR 00E0H PREDEFINED

DAC0H. . . . . . . . . . . . . . D ADDR 00FAH PREDEFINED

DAC0L. . . . . . . . . . . . . . D ADDR 00F9H PREDEFINED

DACCON . . . . . . . . . . . . . D ADDR 00FDH PREDEFINED

DPL. . . . . . . . . . . . . . . D ADDR 0082H PREDEFINED

LED. . . . . . . . . . . . . . . NUMB 00B4H

P3 . . . . . . . . . . . . . . . D ADDR 00B0H PREDEFINED

STEP . . . . . . . . . . . . . . C ADDR 000CH

TABLE. . . . . . . . . . . . . . C ADDR 1000H